EPV Technologies

Newsletter

May 2025

THIS MONTH HIGHLIGHTS

- **z17 Capacity Planning – Part 1**
- **2025 CPU MF IBM z17 Formulas and Updates**
- **EPV Next Generation 2025 report**

z17 Capacity Planning – Part 1

On April 8th IBM announced its new generation of the mainframe. The new system is called IBM z17 while the family model is 9175.

Experienced capacity planners know that every new generation of machines provides a major challenge to their skills. They also know that their best friends are the IBM LSPR benchmarks, the IBM zPCR tool, the Measurement Facility counters provided in SMF 113 and an up-to-date performance database.

Even if the z17 processor cache architecture is similar to z16, there are significant changes and new components that must be carefully analyzed.

In the first part of this paper, we will have a look at the most important capacity characteristics of the IBM z17.
Starting from the IBM LSPR benchmarks, we will then estimate the MIPS capacity of each IBM z17 processor model.
Finally, we will compare z17 single CP capacity and workload variability with previous machine generations.

In the second part we will compare z16 and z17 processor cache architecture. Then we will analyse in more detail the new z17 Measurement Facility basic and extended counters provided in SMF 113, using them to calculate the most important indexes to use in performance analysis and capacity planning.

*If you want to receive this paper, you can reply to this e-mail writing **"z17 Capacity Planning – Part 1"** in the subject.*

2025 CPU MF IBM z17 Formulas and Updates

A detailed IBM presentation providing an update of the most important SMF 113 counters and formulas for the last mainframe generations, from z10 to z17.

Download at: https://www.ibm.com/support/pages/node/6354583

EPV Next Generation 2025 report

The 5th edition of the EPV Next Generation conference has been held on May 20 and 22, 2025.
Amongst many new features available through the normal maintenance, a new

product, MyEPV Dynamic, has been presented.
As usual, many Customers from various Countries participated to the conference and gave positive feedbacks.

If you were unable to attend and are interested in some of the topics presented, please contact us and we will find a way to share the news.

Customer question

Hello, I see three zEDC entries in the Resources menu of EPV for z/OS: ZEDC ACTIVITY, ZEDC SYNCH ACTIVITY and ZEDC ASYNCH ACTIVITY.

ZEDC ACTIVITY is barred; no report is provided.
We can navigate ZEDC ASYNCH ACTIVITY up to ZEDC AS ASYNCH ACTIVITY but we can't for ZEDC SYNCH ACTIVITY.

Can you please clarify?

EPV Technical support answer

ZEDC ACTIVITY is maintained for compatibility only. It provides information about zEDC Express Cards Activity.

With the z15 machine, IBM eliminated the need of the zEDC Express cards by

introducing the Integrated Accelerator for zEDC.
ZEDC ASYNCH and SYNCH ACTIVITY reports provide information about the Accelerator activity.

ZEDC SYNCH ACTIVITY measurements come from SMF 113. No information about address space activity is provided.

ZEDC ASYNCH ACTIVITY measurements at system level come from SMF 74-10 while measurements at address space level come from SMF 30.

Implicit Long Term CPU protection

The first step towards implicit CPU protection has been taken with System Recovery Boost.
While the boost is in effect, CPU protection is automatically assigned to critical work.
Any single-period service class of importance 1 or 2 is considered critical work and is implicitly set as CPU-critical.
Of course, when the boost period ends, the CPU-critical option is reset to the state

defined in the currently active WLM policy.

With z/OS 3.1, a further enhancement has been introduced to protect critical work.
Long term CPU protection is implicitly assigned to critical work also when no boost is in effect.
It is only assigned to single-period service classes and, by default, to the first period of multiperiod service classes.

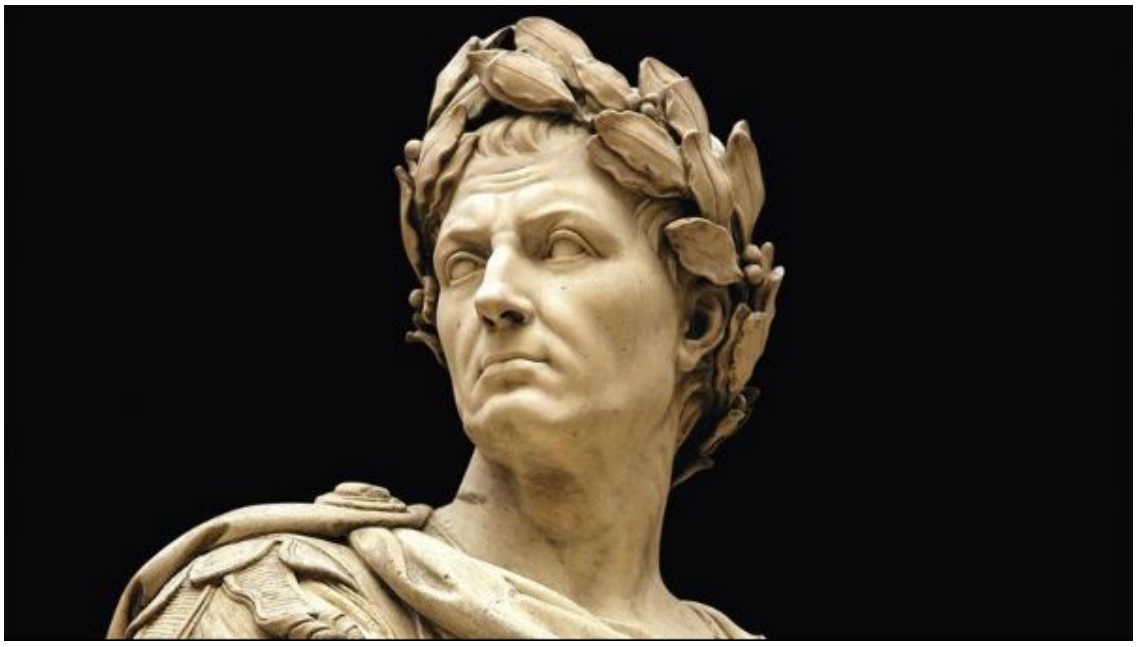
Two new OPT parameters are provided with z/OS 3.1 to define how CPU protection is implicitly assigned to work:

- CCImp; it applies when no boost is active; possible values are 0, 1, 2; default is 1;
- CCImpBoost; it applies during boost periods; possible values are 0, 1, 2; default is 2.

0 means that CPU protection is not implicitly assigned to any work.
1 and 2 define the importance level up to which CPU protection is implicitly assigned to the work.

CPU Critical assigned in the active WLM policy always prevails.

Quotes



"Experience is the teacher of all things."
Julius Caesar

We care about your Privacy. EPV Technologies is GDPR-compliant.

You may have heard about the new General Data Protection Regulation ("GDPR"), that comes into effect May 25, 2018.
It was introduced to unify all EU countries to a unique data regulation, ensuring that all data protection laws are applied identically within the EU.
It also protects EU citizens from organisations using their data irresponsibly and puts them in charge of "what", "where" and "how" information is shared.

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